Semidistributed Model of Millimeter-Wave FET for *S*-Parameter and Noise Figure Predictions

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Abstract—**Besides sophisticated fully distributed FET models for predicting small-signal performance up to millimeter-wave frequencies, it may be convenient to make use of a simpler electrical model which avoids the need of solving coupled differential equations while taking account of propagation effects along device electrodes. We present a new electrical FET model derived from a partition of the actual transistor along its gate width into N identical sections. This so-called sliced model has two main advantages in comparison with distributed models: first, the derivation of its element values is obtained by a direct application of Kirchhoff's laws and, second, insertion of the noise sources is easy and makes it possible to predict the FET noise parameters. An example is given that shows good agreement between minimum noise figures derived from the "sliced" model and from the Fukui formula in the range 18–40 GHz.**

I. Introduction

With the movement to millimeter-wave frequencies and the good performances of FET's up to 60 GHz, sophisticated electrical models have been proposed which include propagation effects along device electrodes considered to be coupled transmission lines [1], [3]. It is true that the transistor dimensions become of the same order of magnitude as the wavelength if the frequency of operation reaches the millimeter-wave range. The FET electrodes are then equivalent to active transmission lines terminated at the end with an open. Decreasing the gate width and increasing the transconductance and the cutoff frequency of the device are nearly opposite objectives. Therefore, with MESFET's operating at several tens of gigahertz, the gate width to wavelength ratio is higher than 10% or 20% and the validity of the common lumped-element modeling is questionable [4], [5].

This paper presents a new electrical FET model derived from a partition of the actual transistor along its gate width into N identical sections. This so-called sliced model presents two main advantages with regard to fully distributed models. First, small-signal performance is derived from a direct application of Kirchhoff's laws and does not require solving coupled differential equations. Second, the insertion of noise sources is easy and makes it possible to predict the FET noise parameters.

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After a short presentation of this model in Section II, noise modeling and noise measurement are exhaustively presented in Sections III and IV respectively. The procedure of FET noise parameter extraction is explained in Section V. Results are then given for minimum noise figure derived either from the "sliced" model or from the Fukui formula in the range 18–40 GHz.

II. The "Sliced" FET Model

As shown in Fig. 1, the transistor model is composed of N identical sections sliced along the actual FET gate width W. Each section (two-port Q with Z_g and Z_d impedances) represents a standard lumped-element model of a common-source MESFET with gate width W/N. Note that the equivalent model neglects any mutual inductances between the gate and drain electrodes.

With the help of matrix relations between the different sections, the admittance matrix (Y_T) of the transistor is established from a direct application of Kirchhoff's laws:

$$\begin{pmatrix} I_{go} \\ I_{do} \end{pmatrix} = (Y_T) \begin{pmatrix} V_{go} \\ V_{do} \end{pmatrix} \tag{1}$$

where the vectors (I_{go}, I_{do}) and (V_{go}, V_{do}) represent the currents and voltages at the FET ports. For more details, see [6].

The integer N is chosen so that the ratio $W/N \cdot \lambda_g$, where λ_g is the propagation wavelength on the device electrodes, is smaller than a few percent. Thus, each section of the actual FET can be represented by the common lumped-element model.

III. Noise Modeling

The "sliced" model is extended to include the two types of noise sources, shown in Fig. 2 for the ith section:

1) intrinsic FET noise sources i_{ng}, i_{nd} with correlation coefficient C;
2) extrinsic noise sources i_{tg}, i_{td}, and i_{ts} related to FET parasitic resistances.

The sources are assumed to be uncorrelated from one section to the other and are characterized by their mean-

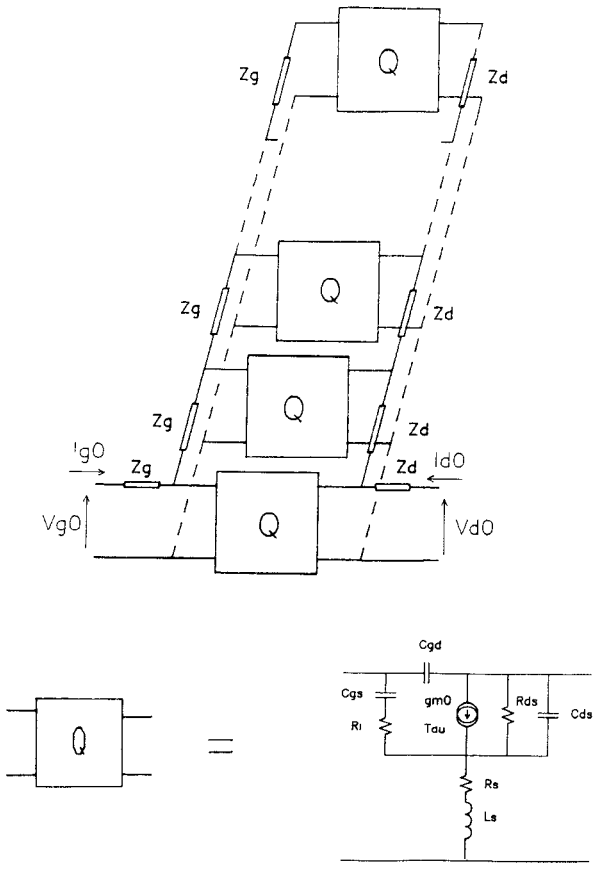

Fig. 1. "Sliced" transistor model.

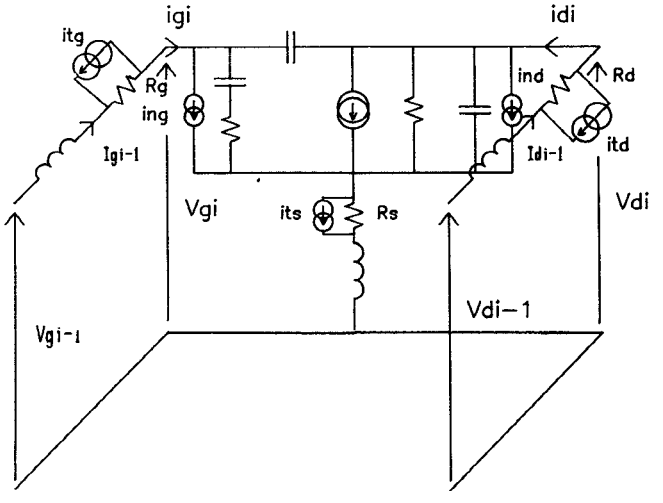

Fig. 2. The ith section of the "sliced" model with noise sources.

squares values [7]:

$$\overline{|i_{ng}|^2} = 4kt_o\Delta f\frac{\omega^2 C_{gs}^2 R}{g_{mo}} \tag{2}$$

$$\overline{|i_{nd}|^2} = 4kt_o\Delta f g_{mo} P \tag{3}$$

$$\overline{|i_{tl}|^2} = 4kt_o\Delta f R_l^{-1} \qquad \text{with } l = g,\ d, \text{ or } s. \tag{4}$$

The coefficients P, R, and C, which are dependent on FET topology and bias conditions, need to be determined from noise measurements. For that, a relation between

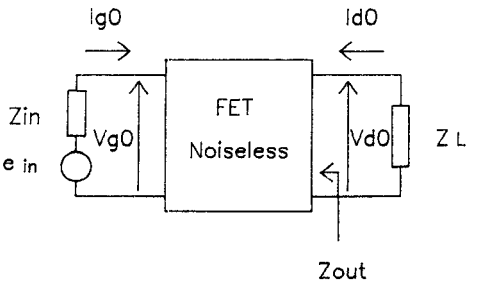

Fig. 3. Noiseless two-port with noisy input termination impedance Z_{in}.

the noise factor, F, the noise sources, and the termination impedance, Z_{in} (admittance Y_{in}), at the FET input is derived from a method similar to that used in Section II. Starting with the FET output conjugate matched, the circuit analysis can be greatly simplified by adding the contribution of different noise sources to the overall available power.

1) The FET is assumed quiet and the contribution of the noisy input termination impedance Z_{in} (admittance Y_{in}) to the available power at the actual drain port is calculated as P_1.
2) The intrinsic FET noise sources i_{ng} and i_{nd} provide the output power P_2.
3) The extrinsic FET noise sources i_{ts} and i_{tg}, i_{td} give the respective contributions P_3 and P_4.

The FET noise factor, F, according to its definition, can be expressed as

$$F = (P_1 + P_2 + P_3 + P_4)/P_1. \tag{5}$$

For clarity, the derivation of these noise powers is given in the Appendix, except for P_1, which can be found with a straightforward manipulation. As shown in Fig. 3, the FET is considered a noiseless two-port terminated at its input by the noise generator e_{in}, defined by the Nyquist formula

$$\overline{|e_{in}|^2} = 4kt_o\Delta f\,\mathrm{Re}(Z_{in}) \qquad (\mathrm{Re} = \text{real part of}).$$

Application of Kirchhoff's laws gives

$$V_{go} = e_{in} - Z_{in}I_{go} \tag{6}$$

$$V_{do} = -Z_L I_{do} \tag{7}$$

where the load impedance, Z_L, is the conjugate of the FET output impedance.

After substituting (6) and (7) into relation (1), the output noise current I_{do} is obtained as

$$I_{do} = \frac{Y_{21T}e_{in}}{\Delta} \tag{8}$$

with

$$\Delta = (1 + Z_{in}Y_{11T})(1 + Z_L Y_{22T}) - Y_{12T}Y_{21T}Z_L Z_{in}. \tag{9}$$

The coefficients Y_{ijT} are admittance matrix elements defined in (1). From (8), an expression for the available

noise power, P_1, is then obtained as

$$P_1 = \frac{1}{2}\,\mathrm{Re}(Z_L)\overline{|I_{do}|^2} = \frac{1}{2}\,\mathrm{Re}(Z_L)|Y_{21T}|^2\overline{|e_{in}|^2}/|\Delta|^2. \quad (10)$$

The contributions of the FET noise sources to the available output power are expressed as follows (see the Appendix for definitions of coefficients K_1 through K_5):

$$P_2 = \frac{1}{2}\,\mathrm{Re}(Z_L)\left\{|K_1|^2\overline{|i_{ng}|^2} + |K_2|^2\overline{|i_{nd}|^2} + 2\,\mathrm{Re}\left(K_1K_2^*\overline{i_{ng}i_{nd}^*}\right)\right\}/|\Delta|^2 \quad (11)$$

$$P_3 = \frac{1}{2}\,\mathrm{Re}(Z_L)|K_3|^2\overline{|its|^2}/|\Delta|^2 \quad (12)$$

$$P_4 = \frac{1}{2}\,\mathrm{Re}(Z_L)\left\{|K_4|^2\overline{|i_{tg}|^2} + |K_5|^2\overline{|i_{td}|^2}\right\}/|\Delta|^2. \quad (13)$$

Using relationships (5), (11), (12), and (13), the FET noise factor, F, is finally obtained as

$$F = 1 + \left\{|K_1|^2\overline{|i_{ng}|^2} + |K_2|^2\overline{|i_{nd}|^2} + 2\,\mathrm{Re}\left(K_1K_2^*\overline{i_{ng}i_{nd}^*}\right) + |K_3|^2\overline{|its|^2} + |K_4|^2\overline{|itg|^2} + |K_5|^2\overline{|itd|^2}\right\} / |Y_{21T}|^2\overline{|e_{in}|^2}. \quad (14)$$

F is seen to depend on

- "sliced" model elements through coefficients K_j;
- termination impedance Z_{in} (admittance Y_{in});
- coefficients P, R, and C through noise currents.

These coefficients need to be determined by fitting the noise factor expressed by (14) with experimental values measured for different impedances Z_{in}. The coefficients K_j are obtained from the (Y_t) matrix elements determined by fitting S-parameter measurements up to 26.5 GHz.

IV. Noise Measurement Technique

The experimental setup is schematically represented in parts (a) and (b) of Fig. 4. Two isolators provide 50 Ω matching to noise source and mixer input. The DUT consists of three parts: the FET chip inserted between two half-test fixtures. The available power is obtained through a proper adjustment of the output tuner. The different input impedances Z_{in} (or reflection coefficients Γ_{in}) are obtained from the input half-test fixture, composed of different stub lengths.

After eliminating the mixer noise by autocalibration, the automatic noise figure meter provides the noise factor, F_m, of the two-port cascade shown in Fig. 4(b). According to the notation used in this figure, the factor F_m, given by the Früs formula, is expressed as

$$F_m = F_1 + \frac{F-1}{G_1} + \frac{F_2-1}{GG_1} \quad (15)$$

from which the FET noise factor is derived:

$$F = G_1F_m - \frac{F_2-1}{G}. \quad (16)$$

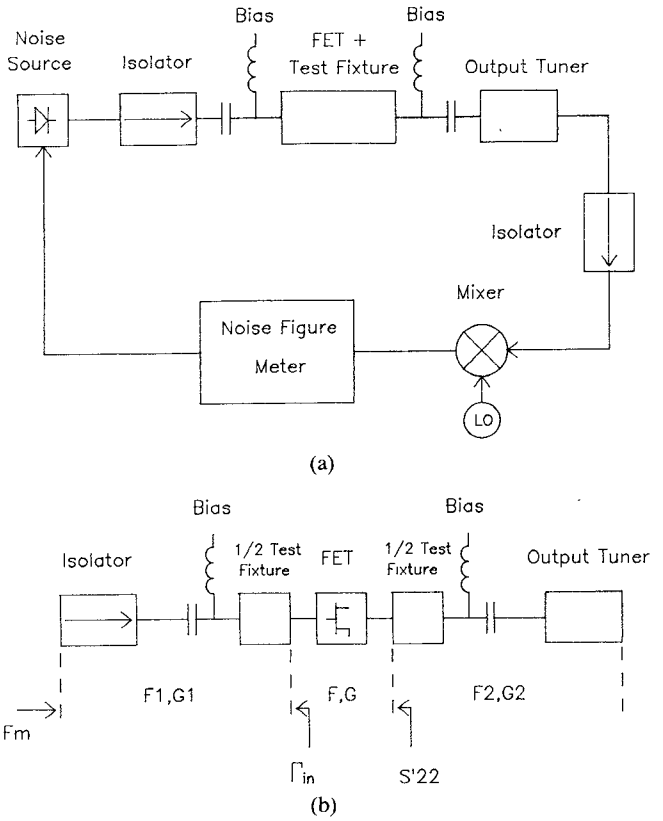

Fig. 4. (a) Experimental setup of noise figure measurement. (b) Simplified block diagram illustrating the measurement principle.

Here G_1 is the available gain of the input stage, composed of the input isolator, bias tee, and half-test fixture, and is given by

$$G_1 = \frac{|S_{21}^1|^2}{1-|S_{22}^1|^2} \quad (17)$$

where S_{21}^1 and $S_{22}^1 = \Gamma_{in}$ are the S parameters for the input stage, measured with an HP 8510 network analyzer. $-F_2$ is the noise figure of the output stage, composed of the output half-test fixture, bias tee, and tuner. Since the output matching two-port is a passive network, $F_2 = 1/G_2$. F_2 is then determined by measuring the output stage losses G_2. The FET available gain, G, can be expressed as

$$G = \frac{|S_{21}|^2}{|1-S_{11}\Gamma_{in}|^2}\,\frac{\left(1-|\Gamma_{in}|^2\right)}{\left(1-|S_{22}'|^2\right.} \quad (18)$$

where

$$S_{22}' = S_{22} + \frac{S_{12}S_{21}\Gamma_{in}}{1-S_{11}\Gamma_{in}}. \quad (19)$$

The coefficients S_{ij} are the S parameters of the FET, measured with the TRL technique [8].

Finally, the FET noise figure, F, is determined for several input impedances Z_{in}.

Extraction of FET Noise Parameters

It is well known that the noise figure, F, of a linear two-port depends on the source admittance ($Y_{in} = G_{in} + jB_{in}$) connected at its input port, according to the follow-

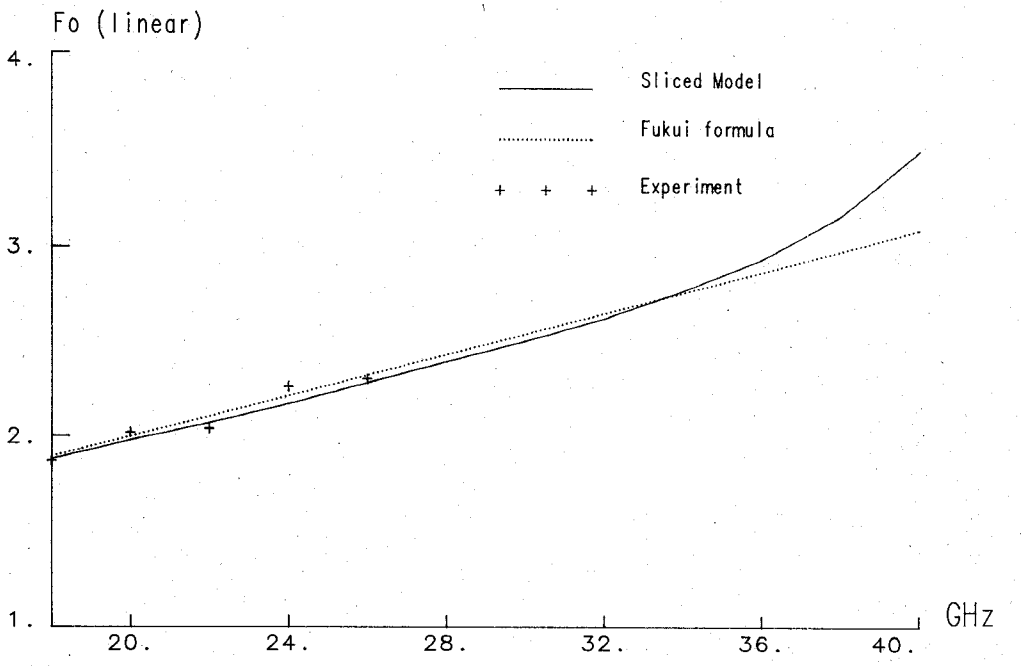

Fig. 5. Minimum noise figure versus frequency from 18 to 40 GHz (bias conditions: $V_{ds} = 3$ V, $I_{ds} = I_{dss}$): + + + + + experimental values; —— "sliced" model ($N = 5$); - - - - - Fukui formula.

ing equation:

$$F = F_o + \frac{R_n}{G_{\text{in}}}\left[(G_{\text{in}} - G_o)^2 + (B_{\text{in}} - B_o)^2\right] \qquad (20)$$

with

F noise figure,
R_n equivalent noise resistance,
F_o minimum noise figure,
$Y_o = G_o + jB_o$: optimum termination admittance that gives minimum noise figure.

In order to estimate the noise parameters, it is necessary to measure the noise figure of the device for more than four values of its input termination admittance (in fact seven values seem to be sufficient [9]). The noise parameters are determined by a least-square fit of expression (20) according to the method described by Mitama and Katoh [10]. This method takes into account the errors in both the noise figure and the input termination admittance measurements.

V. Determination of FET Noise Parameters

In the first step, the coefficients P, R, and C given by (2) and (3) are determined by fitting the noise factor derived from the "sliced" model (eq. (14)) with experimental values. It will be noted that the P, R, and C values are obtained from an averaging process on the noise measurements. Determination of these three coefficients allows us to evaluate the noise factor, F, and derive FET noise parameters.

An alternative form of (20) gives the noise factor, F, as a function of its input termination impedance Z_{in}:

$$F = F_o + \frac{R_n}{R_{\text{in}}}\frac{\left[(R_{\text{in}} - R_o)^2 + (X_{\text{in}} - X_o)^2\right]}{\left(R_o^2 + X_o^2\right)} \qquad (21)$$

with $Z_{\text{in}} = R_{\text{in}} + jX_{\text{in}}$.

Determination of these noise parameters obeys the following steps:

1) Derivation of (14) with respect to R_{in} and X_{in}. Then cancellation of the two expressions $\partial F/\partial R_{\text{in}}$ and $\partial F/\partial Y_{\text{in}}$ gives R_o and X_o.
2) Substitution of R_o and X_o for R_{in} and X_{in} in (14) yields the minimum noise factor, F_o.
3) Computation of F_{50} with $Z_{\text{in}} = 50\ \Omega$ and identification with (21) gives the noise resistance, R_n.

Results are presented in Fig. 5 for minimum noise figure F_o versus frequency ranging from 18 to 40 GHz. Experimental values of F_o have been extracted from noise measurements up to 26 GHz according to the method described in Section IV. Theoretical curves are plotted for the "sliced" model (solid line) and a model derived from the Fukui formula [11] (dashed line):

$$F_o = 1 + K_1\left(\frac{f}{f_T}\right) + K_2\left(\frac{f}{f_T}\right)^2 \qquad (22)$$

with

$$f_T = \frac{g_m}{2\pi C_{gs}}.$$

The lumped model elements of a GaAs Thomson FET (64 μm$\times$0.3 μm) at $V_{ds} = 3$ V and $V_{gs} = 0$ V are as follows: $g_m = 18.5$ mS, $R_i = 3.37\ \Omega$, and $C_{gs} = 0.074$ pF.

The coefficients K_1 and K_2 are determined by fitting (22) with minimum noise figure measurements. Equation (22) is then expressed as

$$F_o = 1 + 1.9\left(\frac{f}{40}\right) + 0.2\left(\frac{f}{40}\right)^2$$

with f in GHz.

Fig. 5 shows good agreement between experimental data and theoretical curves. Propagation effects are negligible up to about 36 GHz, where the deviation between the "sliced" model and the one derived from the Fukui formula is 2.5%. Above 40 GHz, the discrepancy becomes greater than 10% but the FET is then working above its cutoff frequency f_T and perhaps an additional term could be required in (22) for taking the resulting noise increase into account [12].

VI. Conclusion

A new distributed FET model, a so-called sliced FET model, has been presented. It allows the prediction of S parameters up to millimeter-wave frequencies from microwave measurements. In contrast to other recently published electrical models [3], [5], coupled differential equations are replaced by a system of linear equations which are solved by direct application of Kirchhoff's laws. In addition, insertion of noise sources in the small-signal FET model makes it possible to predict the four noise parameters up to 40 GHz from noise figure measurements. The deviation from the Fukui formula in the high part of the 18–40 GHz band represents an interesting feature. This theoretical prediction could be confirmed with further experimental investigation.

Appendix

Derivation of the Available Power P_2, P_3 and P_4

According to Figs. 1 and 2, gate and drain currents at the FET ports are expressed as follows:

$$I_{go} = \sum_{k=1}^{N} i_{gk} \tag{A1}$$

$$I_{do} = \sum_{k=1}^{N} i_{dk} \tag{A2}$$

where the vector (i_{gk}, i_{dk}) represents the currents for the kth two-port Q.

Let us consider Fig. 2 with only *ing* and *ind* noise sources. Application of Kirchhoff's laws leads to the following matrix relation:

$$\begin{pmatrix} i_{gt} \\ i_{dt} \end{pmatrix} = (Y)\begin{pmatrix} V_{gt} \\ V_{dt} \end{pmatrix} + (Ha)\begin{pmatrix} ing \\ ind \end{pmatrix} \tag{A3}$$

where (Y) is the admittance matrix of the two-port Q.

Applying recurrent relations between the different sections, a matrix relation is derived between voltage and current vectors of the first and the ith section:

$$\begin{pmatrix} V_{gt} \\ V_{dt} \end{pmatrix} = (Ai)\begin{pmatrix} V_{go} \\ V_{do} \end{pmatrix} + (Bi)\begin{pmatrix} I_{go} \\ i_{do} \end{pmatrix} + (Ca_i)\begin{pmatrix} ing \\ ind \end{pmatrix} \tag{A4}$$

where (Ai), (Bi), and (Ca_t) are obtained from recurrent relations and are related to the FET model elements.

Substitution of (A3) into (A1) and (A2) gives the following relation:

$$\begin{pmatrix} I_{go} \\ I_{do} \end{pmatrix} = (Y)\begin{pmatrix} V_{g1} + V_{g2} + \cdots + V_{gN} \\ V_{d1} + V_{d2} + \cdots + V_{dN} \end{pmatrix} + N(Ha)\begin{pmatrix} ing \\ ind \end{pmatrix}. \tag{A5}$$

Substitution of (A4) for i ranging from 1 to N into (A5) yields

$$\begin{pmatrix} I_{go} \\ I_{do} \end{pmatrix} = (Y_T)\begin{pmatrix} V_{go} \\ V_{do} \end{pmatrix} + (Na)\begin{pmatrix} ing \\ ind \end{pmatrix} \tag{A6}$$

where (Y_T) is the noiseless admittance matrix of the transistor and (Na) is a "noisy" matrix related to the *ing* and *ind* noise sources:

$$(Na) = (Y)\left|((Ca_1) + (Ca_2) + \cdots + (Ca_N)\right| + N(Ha).$$

Ohm's law applied to (A1) gives

$$V_{go} = -Z_{in} I_{go} \tag{A7}$$

$$V_{do} = -Z_L I_{do}. \tag{A8}$$

The output noise current, I_{do}, is then derived by substituting (A7) and (A8) into (A6):

$$I_{do} = \frac{K_1}{\Delta} ing + \frac{K_2}{\Delta} ind \tag{A9}$$

where Δ is expressed in (9):

$$K_1 = (1 + Z_{in} Y_{11T}) Na_{21} - Y_{21T} Z_{in} Na_{11}$$

$$K_2 = (1 + Z_{in} Y_{11T}) Na_{22} - Y_{21T} Z_{in} Na_{12}.$$

Finally, the output available power P_2 is found as

$$P_2 = \frac{1}{2}\,\mathrm{Re}(Z_L)\frac{1}{|\Delta|^2}\left\{|K_1|^2 \cdot \overline{|ing|^2} + |K_2|^2 \cdot \overline{|ind|^2} + 2\,\mathrm{Re}\left(K_1 K_2^* \overline{ing\, ind^*}\right)\right\}. \tag{A10}$$

Contribution of Rs Thermal Noise

Considering only the noise source i_{ts}, the available power P_3 is now derived. Taking advantage of the circuit symmetry, relations (A1) to (A8) are valid if index a is replaced by index b and the vector (i_{ng}, i_{nd}) by the vector (its, its) throughout.

The following relation can be written:

$$I_{do} = \frac{K_3}{\Delta} i_{ts} \tag{A11}$$

where

$$K_3 = (1 + Z_{in} Y_{11T})(Nb_{21} + Nb_{22}) - Y_{21T} Z_{in}(Nb_{11} + Nb_{12})$$

$$Nb = (Y)[(Cb_1) + \cdots + (Cb_N)] + N(Hb).$$

Then the available power P_3 is obtained as

$$P_3 = \frac{1}{2}\,\mathrm{Re}(Z_L)\frac{|K_3|^2}{|\Delta|^2}\overline{|its|^2}. \tag{A12}$$

Thermal Noise Due to R_g and R_d — Derivation of P_4

Equation (A3) is rewritten as

$$\begin{pmatrix} i_{gi} \\ i_{di} \end{pmatrix} = (Y) \cdot \begin{pmatrix} V_{gi} \\ V_{di} \end{pmatrix} \tag{A13}$$

with

$$V_{gi} = V_{gi-1} - Z_g I_{gi-1} - R_g i_{tg}$$
$$V_{di} = V_{di-1} - Z_d I_{di-1} - R_d i_{td}.$$

From the method set forth at the beginning of the Appendix, a matrix relation can be derived between voltage and current vectors of the first and ith sections:

$$\begin{pmatrix} V_{gi} \\ V_{di} \end{pmatrix} = (A_i) \begin{pmatrix} V_{go} \\ V_{do} \end{pmatrix} + (Bi) \begin{pmatrix} I_{go} \\ I_{do} \end{pmatrix} + (Cci) \begin{pmatrix} i_{tg} \\ i_{td} \end{pmatrix}. \tag{A14}$$

After straightforward manipulation, a relationship is derived for the output current I_{do}:

$$I_{do} = \frac{K_4 i_{tg} + K_s i_{td}}{\Delta} \tag{A15}$$

with

$$K_4 = (1 + Z_{in} Y_{11T}) Nc_{21} - Y_{21T} Z_{in} Nc_{11}$$
$$K_5 = (1 + Z_{in} Y_{11T}) Nc_{22} - Y_{21T} Z_{in} Nc_{12}.$$

If we assume that the two noise sources are uncorrelated, the available power P_4 is finally obtained as

$$P_4 = \frac{1}{2} \mathrm{Re}(Z_L) \frac{1}{|\Delta|^2} \left\{ |K_4|^2 \overline{|itg|^2} + |K_5|^2 \overline{|itd|^2} \right\} \tag{A16}$$

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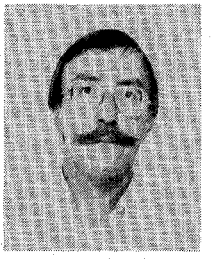

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